# PRODUCT SPECIFICATION

## GQXP-85A4-02D-M(I)

**40GBASE-SR4 Hot Pluggable, VCSEL Connector, MMF, QSFP+ Transceiver,**

## ■ Features:

★ Four-channel full-duplex transceiver module
★ Hot Pluggable QSFP+ form factor
★ Maximum link length of 100m on OM3 Multimode Fiber (MMF) and 150m on OM4 MMF
★ Multirate capability: 1.06Gb/s to 10.5Gb/s per channel
★ Unretimed XLPPI electrical interface
★ Maximum power dissipation <1.5W
★ Reliable VCSEL array technology
★ Extended operating case temperature range: -5° C to 85° C
★ Single 1x12 MPO receptacle
★ RoHS Compliant Part

## ■ Applications:

★ 40GBASE-SR4 40G Ethernet
★ Breakout to 10GBASE-SR Ethernet
★ Proprietary interconnections

## ■ Description:

GQXP-85A4-02D-M(I) transceiver modules are used for 40 Gigabit per second links over multi-mode fiber. They are compliant with the QSFP+ MSA and IEEE 802.3ba 40GBASE-SR4 . Module-level digital diagnostic functions are available via an I2C interface, as specified by the QSFP+ MSA. The optical transceiver is compliant per the RoHS Directive 2011/65/EU.




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## Absolute Maximum Ratings

| Parameter | Symbol | Min. | Typical | Max. | Unit |
|---|---|---|---|---|---|
| Storage Temperature | TS | -40 | | +85 | °C |
| Supply Voltage | VCCT, R | -0.5 | | 3.6 | V |
| Relative Humidity | RH | 0 | | 85 | % |
| Case operating Temperature | TC | -5 | | +85 | ° C |

## Recommended Operating Environment:

| Parameter | Symbol | Min. | Typical | Max. | Unit |
|---|---|---|---|---|---|
| Commercial | TC | 0 | | +75 | °C |
| Industrial | TC | -40 | | +85 | °C |
| Supply Voltage | VCCT, R | +3.14 | 3.3 | +3.47 | V |
| Supply Current | ICC | | | 350 | mA |
| Power Dissipation | PD | | | 1.5 | W |

## Electrical Characteristics ($T_{OP}$ = -5 to 85 °C, VCC = 3.135 to 3.465 Volts)

| Parameter | Symbol | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|
| Data Rate per Channel | | - | 10.5 | | Gbps | |
| Power Consumption | | - | | 1.5 | W | |
| Supply Current | Icc | | | 350 | mA | |
| Transmit turn-on time | | | | 2000 | ms | |
| **Transmitter** | | | | | | |
| Single Ended Output Voltage Tolerance | | -0.3 | | 4 | V | |
| Differential data input swing | Vin, pp | 180 | | 1200 | mVpp | |
| Differential input threshold | | | 50 | | mV | |
| AC common mode input voltage tolerance | | 15 | | | mV | |
| Differential input return loss | | Per IEEE P802.3ba, Section 86A.4.1.1 | | | dB | |
| J2 Jitter Tolerance | | 0.17 | | | UI | |
| J9 Jitter Tolerance | | 0.29 | | | UI | |
| Data Dependent Pulse Width Shrinkage | | 0.07 | | | UI | |
| **Receiver** | | | | | | |
| Single Ended Output Voltage | | 0.3 | | 4 | V | |
| Differential data output swing | Vout,pp | 0 | | 800 | mVpp | |
| AC common mode output voltage (RMS) | | | | | ps | |
| Differential output return loss | | Per IEEE P802.3ba, Section 86A.4.2.1 | | | UI | |
| Output transition time, 20% to 80% | | 28 | | | ps | |
| J2 Jitter output | | | | 0.42 | UI | |
| J9 Jitter output | | | | 0.65 | UI | |
| Power Supply Ripple Tolerance | | 50 | | | mVpp | |




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## Optical Characteristics ($T_{OP}$ = -5 to 85°C, VCC = 3.135 to 3.465 Volts)

| Parameter | Symbol | Min | Typ | Max | Unit | Ref. |
|---|---|---|---|---|---|---|
| **Transmitter** | | | | | | |
| Signaling Speed per Lane | | | 10.5 | | GBd | |
| Center wavelength | | 830 | 850 | 870 | nm | |
| RMS Spectral Width | SW | 30 | - | - | dB | |
| Total Average Launch Power | | - | - | | dBm | |
| Average Launch Power, each Lane | | -7.6 | - | 0 | dBm | |
| Difference in Launch Power between any two Lanes (OMA) | | - | - | 4.0 | dB | |
| Optical Modulation Amplitude, each Lane | OMA | -7.6 | | 2.4 | dBm | |
| Launch Power in OMA minus Transmitter and Dispersion Penalty (TDP), each Lane | | -6.5 | - | | dBm | |
| TDP, each Lane | TDP | | | 3.5 | dB | |
| Extinction Ratio | ER | 3.0 | - | - | dB | |
| Transmitter Eye Mask Definition {X1, X2, X3, Y1, Y2, Y3} | | {0.23, 0.34, 0.43, 0.27, 0.35, 0.4} | | | | |
| Optical Return Loss Tolerance | | - | - | 12 | dB | |
| Average Launch Power OFF Transmitter, each Lane | Poff | | | -30 | dBm | |
| Relative Intensity Noise | Rin | | | -128 | dB/HZ | 1 |
| **Receiver** | | | | | | |
| Signaling Speed per Lane | | | 10.5 | | GBd | |
| Damage Threshold | THd | 3.4 | | | dBm | 1 |
| Average Power at Receiver Input, each Lane | R | -9.5 | | 2.4 | dBm | |
| Receiver Power (OMA), each Lane | | | | 3.0 | dB | |
| Receive Electrical 3 dB upper Cut off Frequency, each Lane | | | | | GHz | |
| RSSI Accuracy | | | | | dB | |
| Receiver Reflectance | Rrx | | | -12 | dB | |
| Stressed Receiver Sensitivity in OMA, each Lane | | - | - | -5.4 | dBm | |
| Receiver Sensitivity(OMA), each Lane | SR | - | - | -9.5 | dBm | |
| Difference in Receive Power between any two Lanes (OMA) | | | | | dB | |
| Receive Electrical 3 dB upper Cutoff Frequency, each Lane | | | | | GHz | |
| LOS De-Assert | LOSD | | | -12 | dBm | |
| LOS Assert | LOSA | -30 | | | dBm | |
| LOS Hysteresis | LOSH | 0.5 | | | dB | |
| Overload | | 2.3 | | | dBm | |




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## Diagnostic Monitoring Interface

Digital diagnostics monitoring function is available on all QSFP+ SR4. A 2-wire serial interface provides user to contact with module. The structure of the memory is shown in flowing. The memory space is arranged into a lower, single page, address space of 128 bytes and multiple upper address space pages. This structure permits timely access to addresses in the lower page, such as Interrupt Flags and Monitors. Less time critical time entries, such as serial ID information and threshold settings, are available with the Page Select function. The interface address used is A0xh and is mainly used for time critical data like interrupt handling in order to enable a one-time-read for all data related to an interrupt situation. After an interrupt, IntL has been asserted, the host can read out the flag field to determine the affected channel and type of flag.

**Lower Memory Map (A0h)**

| Address | Size (Bytes) | Description | Type |
|---|---|---|---|
| 0 | 1 | Identifier | Read-Only |
| 1-2 | 2 | Status | Read-Only |
| 3-21 | 19 | Interrupt Flags | Read-Only |
| 22-33 | 12 | Module Monitors | Read-Only |
| 34-81 | 48 | Channel Monitors | Read-Only |
| 82-85 | 4 | Reserved | Read-Only |
| 86-97 | 12 | Control | Read/Write |
| 98-99 | 2 | Reserved | Read/Write |
| 100-106 | 7 | Module and Channel Masks | Read/Write |
| 107-118 | 12 | Reserved | Read/Write |
| 119-122 | 4 | Reserved | Read/Write |
| 123-126 | 4 | Reserved | Read/Write |
| 127 | 1 | Page Select Byte | Read/Write |

**Upper Memory Map Page 03h**

| Address | Size (Bytes) | Description | Type |
|---|---|---|---|
| 128-175 | 48 | Module Thresholds | Read-Only |
| 176-223 | 48 | Reserved | Read-Only |
| 224-225 | 2 | Reserved | Read-Only |
| 226-239 | 14 | Reserved | Read/Write |
| 240-241 | 2 | Channel Controls | Read/Write |
| 242-253 | 12 | Reserved | Read/Write |
| 254-255 | 2 | Reserved | Read/Write |

**Serial ID: Data Fields**

| Address | Size (Bytes) | Name | Description of Base ID Field |
|---|---|---|---|
| **Base ID fields** | | | |
| 128 | 1 | Identifier | Identifier Type of serial Module |
| 129 | 1 | Ext. Identifier | Extended Identifier of Serial Module |
| 130 | 1 | Connector | Code for connector type |
| 131-138 | 8 | Specification compliance | Code for electronic compatibility or optical compatibility |
| 139 | 1 | Encoding | Code for serial encoding algorithm |
| 140 | 1 | BR, nominal | Nominal bit rate, units of 100 MBits/s |
| 141 | 1 | Extended Rate select Compliance | Tags for extended rate select compliance |
| 142 | 1 | Length(SMF) | Link length supported for SMF fiber in km |
| 143 | 1 | Length(OM3 50um) | Link length supported for EBW 50/125um fiber (OM3), units of 2m |
| 144 | 1 | Length(OM2 50um) | Link length supported for 50/125um fiber (OM2), units of 1m |
| 145 | 1 | Length(OM1 62.5 um) | Link length supported for 62.5/125um fiber (OM1), units of 1m |
| 146 | 1 | Length (Copper) | Link length of copper or active cable, units of 1m |
| 147 | 1 | Device tech | Device technology |
| 148-163 | 16 | Vendor name | QSFP+ vendor name(ASCII) |
| 164 | 1 | Extended Module | Extended Module codes for InfiniBand |
| 165-167 | 3 | Vendor OUI | QSFP+ vendor IEEE company ID |
| 168-183 | 16 | Vendor PN | Part number provided by QSFP+ vendor(ASCII) |
| 184-185 | 2 | Vendor rev | Revision level for part number provided by vendor (ASCII) |
| 186-187 | 2 | Wave length or Copper Cable Attenuation | Nominal laser wavelength (wavelength=value/20 in nm) |
| 188-189 | 2 | Wavelength tolerance | Guaranteed range of laser wavelength(+/- value) from nominal wavelength. (wavelength Tol.=value/200 in nm) |
| 190 | 1 | Max case temp. | Maximum case temperature in degrees C |
| 191 | 1 | CC_BASE | Check code for base ID fields (addresses 128-190) |
| **Extended ID fields** | | | |
| 192-195 | 4 | Options | Rate Select, TX Disable, TX Fault, LOS |
| 196-211 | 16 | Vendor SN | Serial number provided by vendor (ASCII) |
| 212-219 | 8 | Date Code | Vendor's manufacturing date code |
| 220 | 1 | Diagnostic Monitoring Type | Indicates which types of diagnostic monitoring are implemented (if any) in the Module. Bit 1,0 Reserved |
| 221 | 1 | Enhanced Options | Indicates which optional enhanced features are implemented in the transceiver. |
| 222 | 1 | Reserved | |
| 223 | 1 | CC_EXT | Check code for the Extended ID Fields (addresses 192-222) |
| **Vendor Specific ID Fields** | | | |
| 224-255 | 32 | Vendor Specific EEPROM | |

Page02 is User EEPROM and its format decided by user.

The detail description of low memory and page00.page03 upper memory please see SFF-8436 document.




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## Timing for Soft Control and Status Functions

| Parameter | Symbol | Max | Unit | Conditions |
|---|---|---|---|---|
| Initialization Time | t_init | 2000 | ms | Time from power on1, hot plug or rising edge of Reset until the module is fully functional2 |
| Reset Init Assert Time | t_reset_init | 2 | μs | A Reset is generated by a low level longer than the minimum reset pulse time present on the ResetL pin. |
| Serial Bus Hardware Ready Time | t_serial | 2000 | ms | Time from power on1 until module responds to data transmission over the 2-wire serial bus |
| Monitor Data Ready Time | t_data | 2000 | ms | Time from power on1 to data not ready, bit 0 of Byte 2, deasserted and IntL asserted |
| Reset Assert Time | t_reset | 2000 | ms | Time from rising edge on the ResetL pin until the module is fully functional2 |
| LPMode Assert Time | ton_LPMode | 100 | μs | Time from assertion of LPMode (Vin:LPMode =Vih) until module power consumption enters lower Power Level |
| IntL Assert Time | ton_IntL | 200 | ms | Time from occurrence of condition triggering IntL until Vout:IntL = Vol |
| IntL Deassert Time | toff_IntL | 500 | μs | toff_IntL 500 μs Time from clear on read3 operation of associated flag until Vout:IntL = Voh. This includes deassert times for Rx LOS, Tx Fault and other flag bits. |
| Rx LOS Assert Time | ton_los | 100 | ms | Time from Rx LOS state to Rx LOS bit set and IntL asserted |
| Flag Assert Time | ton_flag | 200 | ms | Time from occurrence of condition triggering flag to associated flag bit set and IntL asserted |
| Mask Assert Time | ton_mask | 100 | ms | Time from mask bit set4 until associated IntL assertion is inhibited |
| Mask De-assert Time | toff_mask | 100 | ms | Time from mask bit cleared4 until associated IntlL operation resumes |
| ModSelL Assert Time | ton_ModSelL | 100 | μs | Time from assertion of ModSelL until module responds to data transmission over the 2-wire serial bus |
| ModSelL Deassert Time | toff_ModSelL | 100 | μs | Time from deassertion of ModSelL until the module does not respond to data transmission over the 2-wire serial bus |
| Power_over-ride or Power-set Assert Time | ton_Pdown | 100 | ms | Time from P_Down bit set 4 until module power consumption enters lower Power Level |
| Power_over-ride or Power-set De-assert Time | toff_Pdown | 300 | ms | Time from P_Down bit cleared4 until the module is fully functional3 |

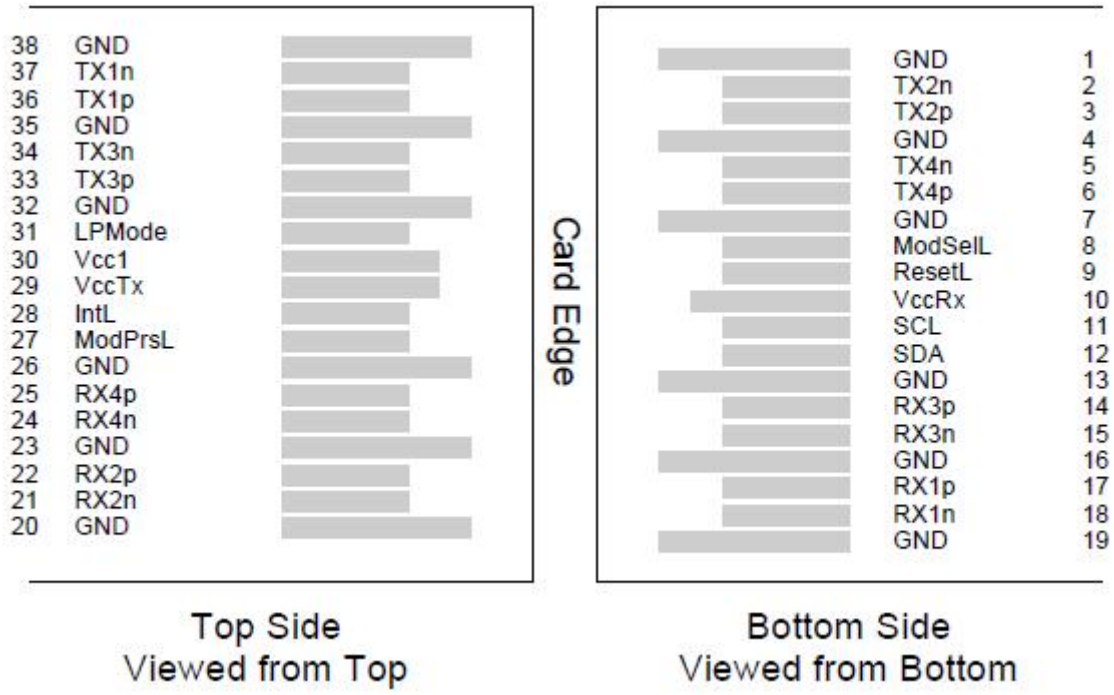
**Note:**

1. Power on is defined as the instant when supply voltages reach and remain at or above the minimum specified value.
2. Fully functional is defined as IntL asserted due to data not ready bit, bit 0 byte 2 de-asserted.
3. Measured from falling clock edge after stop bit of read transaction.
4. Measured from falling clock edge after stop bit of write transaction.

## Pin Function Definitions

| Pin | Logic | Symbol | Name/Description | Ref. |
|---|---|---|---|---|
| 1 | | GND | Ground | 1 |
| 2 | CML-I | Tx2n | Transmitter Inverted Data Input | |
| 3 | CML-I | Tx2p | Transmitter Non-Inverted Data output | |
| 4 | | GND | Ground | 1 |
| 5 | CML-I | Tx4n | Transmitter Inverted Data Output | |
| 6 | CML-I | Tx4p | Transmitter Non-Inverted Data Output | |
| 7 | | GND | Ground | 1 |
| 8 | LVTTL-I | ModSelL | Module Select | |
| 9 | LVTTL-I | ResetL | Module Reset | |
| 10 | | VccRx | +3.3V Power Supply Receiver | 2 |
| 11 | LVCMOS-I/O | SCL | 2-Wire Serial Interface Clock | |
| 12 | LVCMOS-I/O | SDA | 2-Wire Serial Interface Data | |
| 13 | | GND | Ground | 1 |
| 14 | CML-O | Rx3p | Receiver Inverted Data Output | |
| 15 | CML-O | Rx3n | Receiver Non-Inverted Data Output | |
| 16 | | GND | Ground | 1 |
| 17 | CML-O | Rx1p | Receiver Inverted Data Output | |
| 18 | CML-O | Rx1n | Receiver Non-Inverted Data Output | |
| 19 | | GND | Ground | 1 |
| 20 | | GND | Ground | 1 |
| 21 | CML-O | Rx2n | Receiver Inverted Data Output | |
| 22 | CML-O | Rx2p | Receiver Non-Inverted Data Output | |
| 23 | | GND | Ground | 1 |
| 24 | CML-O | Rx4n | Receiver Inverted Data Output | |
| 25 | CML-O | Rx4p | Receiver Non-Inverted Data Output | |
| 26 | | GND | Ground | 1 |
| 27 | LVTTL-O | ModPrsL | Module Present | |
| 28 | LVTTL-O | IntL | Interrupt | |
| 29 | | VccTx | +3.3V Power Supply Transmitter | 2 |
| 30 | | Vcc1 | +3.3V Power Supply | 2 |
| 31 | LVTTL-I | LPMode | Low Power Mode | |
| 32 | | GND | Ground | 1 |
| 33 | CML-I | Tx3p | Transmitter Inverted Data Output | |
| 34 | CML-I | Tx3n | Transmitter Non-Inverted Data Output | |
| 35 | | GND | Ground | 1 |
| 36 | CML-I | Tx1p | Transmitter Inverted Data Output | |
| 37 | CML-I | Tx1n | Transmitter Non-Inverted Data Output | |
| 38 | | GND | Ground | 1 |

## Pin Assignment:




**QSFP+ Transceiver Pad Layout**

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